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New approach to Design of Reversible BCD Adder

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Abstract

Over the last few decades, research in reversible logic has increasingly become very popular and it is gaining greater momentum in the present word. Reversible logic has started finding concert applications in quantum computing, optical computing, nano-technology based system, low-power CMOS design, VLSI design. The principal objective of this work is to argue for quantum implementation of various reversible logic gates by using C-NOT, Controlled-V and Controlled-V^{+} *gates. The present work presents Binary coded decimal adder (BCD) in terms of number of gates, garbage outputs, quantum cost, delay and hardware complexity compared to existing design.*

Keywords: Parallel adder/subtractor, Quantum cost, Reversible logic, and Reversible BCD adder.

1. Introduction

The advancement in fabrication process and high levelintegration has enabled in better logic circuits and energy loss has also been dramatically reduced over the last decades. In the logic computations,heat reduction also has its physical limit. According to Landauer [1, 2] in logic computation every irreversible bit of information loss generates KTln2 joules of heat energy. Where K is Boltzmann's constant of $1.38x10^{-23}$J/K and T is absolute temperature. At room temperature, the heat dissipation is around $2.9x10^{-21}$ J. Energy loss due to Landauer limit is also important as the growth of heat generation causing information loss will be noticeable in future. Reversible circuits are fundamentally different from irreversible circuits. In reversible logic, no information is lost, i.e. the circuit that does not lose information is reversible. Bennett [3] showed that zero energy dissipation would be possible if the circuit consists of reversible gates only. Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. Thus reversibility will be an essential property for the future circuit design. Quantum computation is also gaining popularity as some exponentially hard problems can be solved in polynomial time [4]. Furthermore, reversible circuits are of major interest in optical computing, low power design, quantum computing and nanotechnology based systems. It is not possible to realize quantum computing without reversible logic. If the circuit (gate) is reversible there is one-to-one correspondence between the inputs and outputs. Thus any reversible gates have the same number of inputs and outputs. Neither feedback nor fan-out is allowed in reversible logic [5, 6]. Therefore synthesis of reversible logic design is different from irreversible logic design. One of the major constrains in reversible logic design is to minimize the number of reversible gates used and garbage output produced it. Garbage output refers to the output, but it is not actual output. Therefore it is not used for further computations [7].

To construct reversible gates should have the following features [8]

1. Use minimum input constants
2. Use minimum number of gates
3. Keep the length of cascading gates minimum
4. Use minimum number of garbage outputs

In this research reversible HNG logic gate is used. This paper presents parallel adder/subtractor (with over flow detection), BCD adder, Nine's complement subtraction with less number of reversible gates and garbage outputs.

This paper organized as follows: Section 2 provides the necessary back ground on reversible logic, quantum cost calculation for different gates. Section 3 provides efficient technique for implementation of parallel adder/subtractor (over flow detection), BCD adder, and Nine's complement subtraction has overcome the limitations of the existing methods for designing the proposed system in terms of number of gates and garbage outputs.

2. Reversible and Quantum Gates

2.1 Different reversible logic gates

There are number of reversible gates such as Feynman gate (FG), Toffoli gate (TG), Fredkin gate (FRG), New gate (NG), New Toffoli gate (NTG), HNFG, HNG].

A controlled NOT gate is also known as 2x2 Feynman (FG) gate, A, B are inputs , P,Q are outputs as shown in Fig.1. It performs Exclusive-OR between two inputs; but in this case, one extra output will be generated which is called garbage output. FG gate implements the logic function P=A, and Q=A B. Feynman gate is a suitable gate for a single copy of a bit. If B=0, input A will copy in both outputs i.e P=A, Q=A shown in Fig.2. Thus Feynman gate is most suitable gate for single copy of bit. Since the garbage output does not produced.

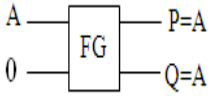
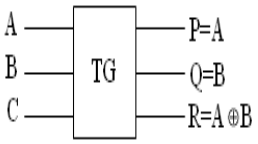


Fig.1.FG gate Fig.2. FG as copying gate

3x3 Toffoli (TG) gate inputs are A, B, C and outputs are P, Q, R as shown in Fig.3. TG gate plays an important role in reversible logic synthesis. TG gate can be considered as universal reversible gate. Any Boolean function will be implemented by using TG gate.



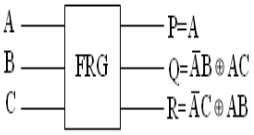
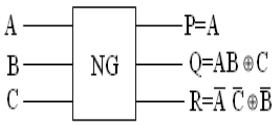


Fig.3.Toffoligate Fig.4.Fredkin gate

3x3 Fredkin (FRG) gate is shown in Fig.4. Inputs are A, B, C and outputs are P, Q, R. In reversible literature, FRG gate place has its importance as it is one through gate (one input is directly generated as output) and also two other inputs can generate two Boolean functions. If A=0 then outputs P, Q are simply generate two Boolean functions. Otherwise if A=1, then the other two input lines (b and C) are swapped.



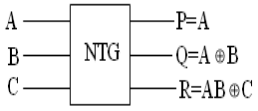
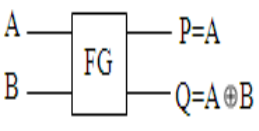


Fig.5.Newgate Fig.6.New Toffoli gate

3x3 New (NG) gate is shown in Fig.5. The inputs are A, B, C and outputs are P, Q, and R.

3x3 New Toffoli (NTG) gate is shown in Fig.6. The inputs are A, B, C and outputs are P, Q, and R.TG is also known as Peres (PG) gate. Actually the PG is the combination of TG and FG, so it can generate two output functions simultaneously.

4x4 MTSG gate is shown in Fig.7(a). The modified TSG gate is a MTSG gate. Let us consider the inputs as A, B, C and D and the outputs are P, Q, R and S. Individually the outputs are P=A, Q=A ⊕B, R=A ⊕B ⊕C, S=(A⊕ B)C⊕ AB ⊕ D. MTSG gate singly acts as full adder, if C=Cin, D=0 as shown in Fig.7(b).



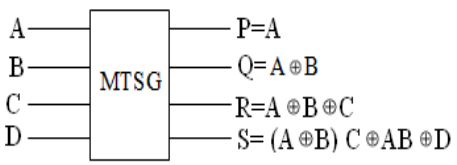


Fig.7(a): MTSG gate

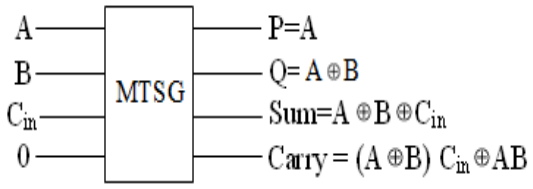


Fig.7(b): MTSG gate as full-adder

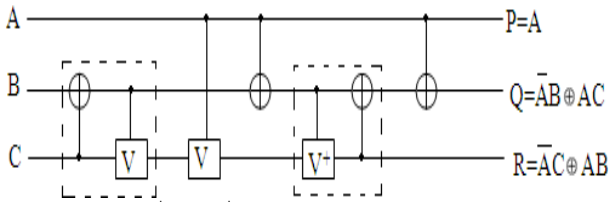
2.1.1Quantum analysis of different reversible logic gates

Calculating quantum cost is always an interesting topic in reversible circuit. Most common applications of quantum theory are Quantum circuits, nano technologies, DNA technologies, optical computing. Every reversible gate can be calculated in terms of quantum cost and hence every reversible circuit can be measured in terms of Quantum cost. Reducing the quantum cost from reversible circuit is always a challenging one and researches are still going on this area.

The quantum cost of any reversible 2x2 gates is taken as unity. The quantum cost of all reversible 1x1 gates is assumed as zero. The 1x1 reversible gates is NOT gate. Thus quantum cost of all reversible gates is realized by using 1x1 NOT gates 2x2 reversible gates. 2x2 reversible gates are V and V+ as shown in Fig. 8 and 9. (V is square root of NOT gate and V+ is its Hermitian) and controlled NOT gate.

The V and V+ quantum gates have the following properties.

V x V = NOT



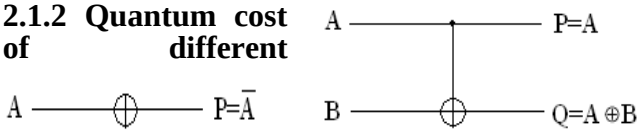
V x V^+ = V^+ x V = I (Identity)

V x V = NOT

The quantum cost of any reversible gates can be calculated by counting the number of CNOT gate ,V and V+.

Fig.8.Controlled V gateFig.9.Controlled V^+ gate

2.1.2 Quantum cost of different reversible logic gates

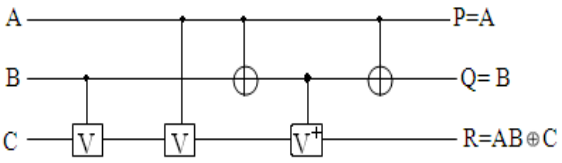


Reversible NOT gate: Reversible NOT gate is 1 x 1 gate as shown in Fig. 10. The quantum cost is 0.

Fig.10.NOT gate Fig.11. Quantum FG gate

Feynman gate: CNOT is also called as 2 x 2 FG gate. FG gate is one through because it passes one of its inputs. Every linear function can be built by using only 2 x 2 FG and inverters. Quantum cost of FG gate is 1. Quantum equivalent circuit of FG gate is shown in Fig.11

Toffoli gate: Fig .12 shows the quantum equivalent realization of three-input TG gate. The quantum cost of the TG gate is 5 (V is a square-root-of NOT gate and V^+ is its Hermitian.Thus VV creates a unitary matrix of NOT gate and VV^+ creates a identity matrix (an identity matrix, just



describing a quantum wire).

Fig.12. Quantum eguivalent of Toffoli gate

Fredkin gate:Fig.13. shows the quantum equivalent realization of three-input FRG gate. The quantum cost of the FRG gate is five (same as TG gate). Each dotted rectangle in Fig.13 isequivalent to 2x2 FG gate for that particular case cost is one.

Fig.13. Quantum eguivalent of Fredkin gate

MTSG gate:Fig.14. shows the quantum equivalent realization of four -input MTSG gate. The quantum cost of the MTSG gate is five.

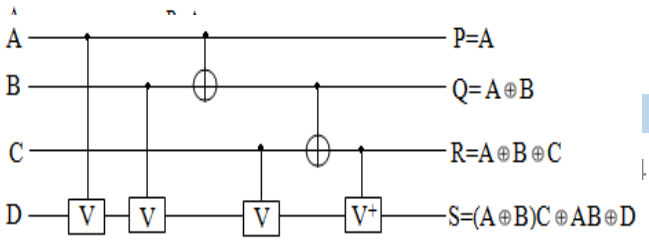


Fig.14 : Quantum equivalent of MTSG gate

3. 4-bit Ripple Carry Adder

4-bit Ripple Carry Adder: The basic building block of ripple carry adder is the full adder. Binary adders are implemented to add two numbers. So 4 Full -Adders are required to add two 4-bit binary numbers. The reversible ripple carry adder can be designed by cascading the reversible full adder. In this work, 4-bit ripple carry is designed by cascading 4- MTSG gates as shown in Fig.15. The output expressions for the ripple carry adder are**:**

$$S_i = A \oplus B \oplus C_i$$

and $C_{i+1} = (A \oplus B)\, C_i \oplus AB$

Where (i=0, 1, 2 ...)

The ripple carry adder is designed with minimum number of reversible gates, garbage output, quantum cost and total logical calculations.

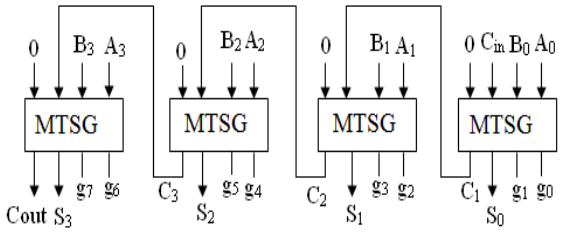


Fig.15. 4-bit Reversible Ripple carry adder

4. Proposed BCD adder

A reversible BCD adder consists of three components: a 4-bit parallel adder, overflow detection logic and overflow correction logic.

In Ref. [10], two 4-bit parallel adders, which was a direct methodology. There are two parallel adders, the output of first 4-bit parallel adder which is the partial sum of two BCD numbers, is provide for to the error detection circuit. The error detection circuit is also a conventional one and no minimization was existing in the error detection expression ((T2 + T1)T3+C4). When adding two BCD numbers, the maximum sum is 18. This means that ((T2 + T1)T3) and C4 cannot be true at the same time. Therefore, the error detection expression F can be computed using an Exclusive OR instead of an OR operation. After that, another 4-bit parallel adder is working to get finial output. Because of using the AND-OR expression for error correction logic and 4-bit parallel adder in the error correction logic, the design needs large number of gates and automatically complexity is increases.

The proposed design approach is shown in Fig.16. In order to propose the 1-digit BCD adder, we have proposed three logics termed as by adding two BCD digits, Overflow Detection and Overflow Correction generated circuit.

In the design of reversible BCD adder, the primary concern is to keep the number of gates and number of garbage outputs as minimum as possible. As the number of gates is reduced, it is much likely that delay will also be reduced garbage output is another important criterion. Circuits which less number of garbage outputs are always desirable Several lower bounds for reversible BCD Adder in terms of number of gates and garbage outputs are presented in this paper.

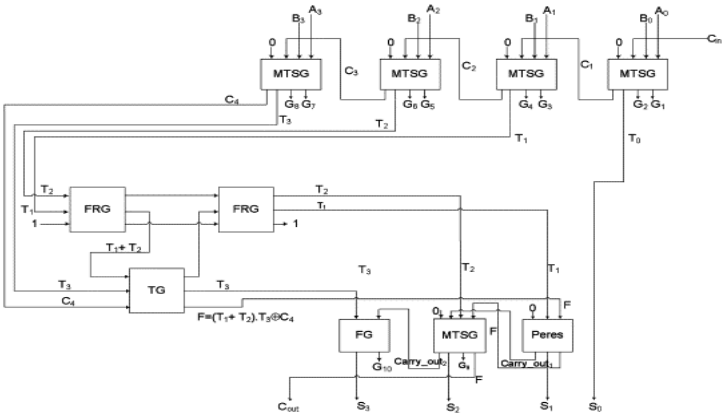


Fig.16. Proposed Reversible BCD adder

5. Conclusion

In this paper, we proposed reversible BCD adder using reversible gates. In this design we used reversible full-adder circuit, it requires only one reversible gate such as MTSG gate and it produces two garbage outputs. The proposed reversible full adder is better than the previous reversible full adders. We applied the new reversible full adder to the design of a 4-bits reversible parallel adder. The proposed reversible BCD adder circuit using 1 parallel adder with error detection and correction circuit. The proposed design has all the good features of reversible logic synthesis.

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