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Efficient Low-Power SR Flip-Flop Design with On/Off Control

Ajay Sharma[1], Abhishek[2], Nitin Singh Singha[3], Kamal Singh[4]

[1, 2] PG Student, Electronics and communication, National institute of technology Delhi, India.

[3] Assistant Professor, Electronics and communication, National institute of technology Delhi, India.

[4] Research Scholar, Electronics and communication, National institute of technology Delhi, India.

Emails: *ajaysharma1626@gmail.com[1],1998abhishek1009@gmail.com[2], nitinsingha@gmail.com[3], kamal.rana13116@gmai.com[4]*

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Abstract

Fundamental to logic circuit construction, metal oxide semiconductor (MOS) devices serve as the foundational components. The growing demands of consumers in the electronics sector are heightened by technological advancements. The utilization of nano-scale technology presents a myriad of challenges for integrated circuit (IC) designers, as no single technology comprehensively meets all requirements. The essential requirement has evolved to demand superior performance coupled with minimal power dissipation and heightened stability. Achieving low power consumption in VLSI devices is crucial for optimal efficiency. With the escalating demand for compact electronic components and devices, the electronics industry has experienced rapid growth over the past few decades. The world and technology are advancing in tandem, with an increasing demand for compact, highly efficient devices. In response to this demand, flip-flops have emerged, finding numerous applications in electronics, including their use in devices and laptops. Reducing the dimensions of flip-flops introduces challenges related to leakage current, hindering the design of low-power circuits. Addressing this issue in SR flip-flops, this paper introduces an approach referred to as OFF/ON. The realization of ONOFIC in SR flip-flops effectively mitigates leakage currents, transforming the flip-flop into a low-power consumption component.

1. Introduction

The industry is advancing concurrently. With escalating demand for compact and highly efficient devices, flip-flops have emerged as a consequential outcome. These flip-flops find myriad applications in electronics, and presently, they find widespread use in activities like digital signal processing [1]. The flip-flop stands as a primary hardware device extensively employed in synchronous FSM [2]. Among its various applications, the SR flip-flop plays a significant role, including its use in addressing and eliminating mechanical bounce [3]. Flip-flops come in both simple and clocked Variations [4]. They exhibit positive edge triggering, implying that data is accepted from the input when the clock is rising. Additionally, they demonstrate negative edge triggering, signifying that data is sampled when the clock is falling. Logic circuits are generally classified into two main types: combinational and sequential logic circuits. Combinational logic circuits produce their output based solely on the present input values, whereas sequential logic circuits rely on both the current input values and the preceding input values. Among various flip-flops, the SR flip-flop, short for Set-Reset flip-flop, is notably simpler. In the SR flip flop there is two input & a clock signal which are rest & set. A set input set to a high level yields a high output, while a reset input set to a high level results in a low output. If both set and reset inputs

are elevated, the output enters an invalid state. The interconnection of NOR and NAND gates through simple cross-coupling is employed for this purpose. The ongoing trend in the electronics field involves the continuous scaling down of technology due to the widespread use of small devices. The process of scaling technology brings numerous benefits, enabling the creation of increasingly smaller devices such as modern iPods, tablets, pacemakers, and hearing aids. However, there is a trade-off, as scaling also entails a challenge in maintaining low-power properties. The demand for small devices remains high, emphasizing the crucial need for low power dissipation in these contemporary times. The chip's maximum power consumption is contingent upon its implementation and the technology employed [5]. Short channel refers to reduced channel length in transistors, while thin gate oxide implies thinner insulating layers, enhancing transistor performance [6]. CMOS scaling is the continuous reduction of transistor dimensions in complementary metal-oxide-semiconductor technology. This process enhances device performance, reduces power consumption, and increases circuit density, enabling the development of smaller and more efficient electronic devices [7]. Lowering the input voltage leads to an augmentation in sub-threshold leakage current, while a reduction in oxide thickness contributes to an escalation in junction tunnelling of electrons. Significantly decreasing gate oxide thickness enhances transistor performance but increases susceptibility to leakage currents and reliability issues like gate oxide breakdown. [8]. The scaling process is directly associated with electron tunnelling, presenting considerable challenges for emerging standard CMOS SOCs as it leads to elevated current leakage. These leakage currents have a profound impact, as they lead to substantial power consumption, representing a major hurdle in VLSI design. Leakage current is the unintended flow of electric current in a circuit, often occurring due to imperfect insulation or isolation. It results from small currents leaking through unintended paths, posing challenges in high-precision electronics. Engineers employ measures like insulation and shielding to mitigate potential issues and ensure system reliability. [9] In this research paper, a CMOS SR flip-flop is presented, incorporating an ONOFIC design that efficiently alleviates leakage and dissipation to a significant degree. A comparative analysis is performed among the standard SR flip-flop and our CMOS SR flip-flop featuring ONOFIC implemented, with a specific emphasis on power consumption. The paper is organized into different parts. Part 2 explores the relevant literature and explains the ON/OFF (ONOFIC) approach employed in the design of CMOS SR. Section 3 elucidates both the traditional CMOS SR flip-flop and the implement using ONOFIC, while Section 4 presents the results and conclusions. All simulations were conducted using the Cadence tool at the forty-five nm technology node.

2. Review of Existing Literature

The Methods sections should be brief, but they should include sufficient technical information to allow the experiments to be repeated by a qualified reader. Only new methods should be described in detail. Cite previously published procedures in References.

3. Approach Employing On/Off (Onofic)

In the design using the ONOFIC approach, a logic design consisting of pull up as PMOS and pull down as NMOS is design. The particular logic circuits, called as the ON/OFF logic circuits, commonly employs PMOS as the pull-up element and NMOS as the pull-down element. This choice is made because NMOS facilitates a transition to zero, while PMOS facilitates a transition to VDD, allowing for maximum signal swing. Reversing the positions of pull-up and pull-down components would necessitate compromises on specific output factors. This method is marked by its simplicity, involving the addition of just one logic block among the pull-up and pull-down networks. The PMOS and NMOS components need to function in both ON and OFF states for any logic output. This model uses the concept of stacking force to provide maximum resistance and minimum resistance at the incident, thereby reducing current flow. The schematic depicts an ONOFIC approach, where these two transistors are required to be either in a state or a linear state, contingent upon the output logic. This Figure 1 showcases the unique connection of ONOFIC transistors. The NMOS gate is attached to the PMOS drain and the PMOS source is attached to voltage. Additionally, the gate of PMOS is connected to the output. Compatibility of ONOFIC transistors use to reduce dissipation [10].

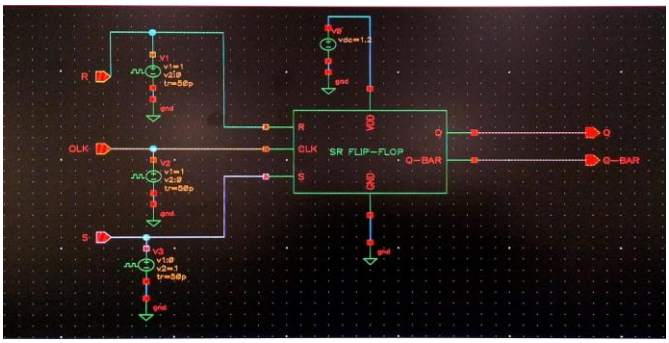

Figure 1 Diagram Illustrating the NETLIST of SR Flip-Flop

4. Completion of CMOS SR Flip-Flops in Conventional and ON/OF Configurations

The diagram (Figure 2) below shows the design of an SR flip-flop using a NOR-based configuration. This chapter focuses on the design of SR flip-flops using CMOS technology, which has the advantages of low power consumption, delay, and performance operating at higher frequency [11]. Another advantage of MOSFETs is that they keep current consumption almost zero when idle. [12].

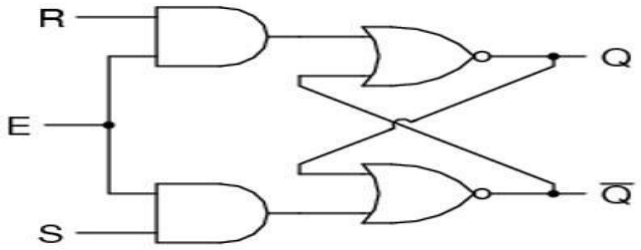

Figure 2 SR Flip-Flop Utilizing NOR Gates

The standard CMOS SR flip-flop consists of just twelve transistors. In this configuration, with the clock signal at a low state, the N tree has two open series terminals, while concurrently, two parallel transistors are in the ON state in the P tree. This configuration allows state to be stored in storage volumes. Instead, when the signal of clock is high, the design turns into a CMOS NOR latch that responds to the S and R inputs are shown in Figure 3.

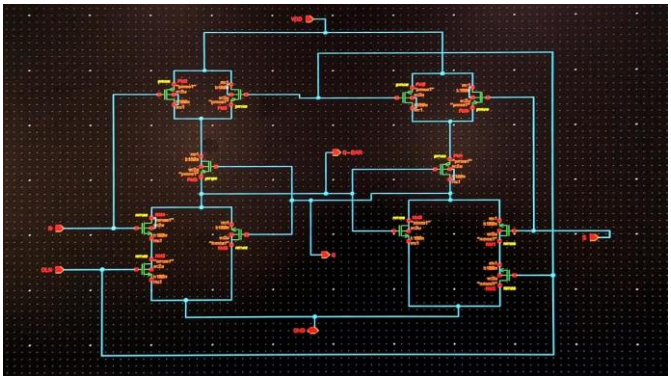

Figure 3 Conventional CMOS SR Flip-Flop

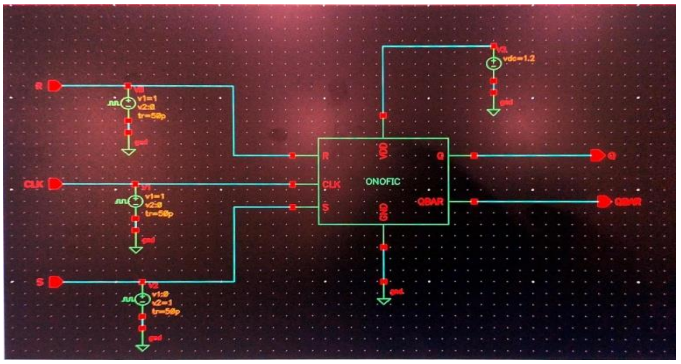

Figure 4 Diagram Illustrating the NETLIST of ONOFIC

The diagram (Figure 4) demonstrates the ONOFIC implementation of an SR flip-flop, showcasing both the conventional CMOS SR flip-flop and the supplementary ONOFIC logic block. This implementation incorporates two logic blocks among the pull-ups and pull-down networks, resulting in a sum of sixteen transistors. The inclusion of four extra transistors in this implementation aids in maximizing performance and efficiency in the design. The functioning of NMOS transistors is controlled by PMOS transistors. In its OFF state, this circuit introduces high impedance, thereby efficiently minimizing leakage currents. This is particularly advantageous during scaling, where leakage currents tend to increase substantially.

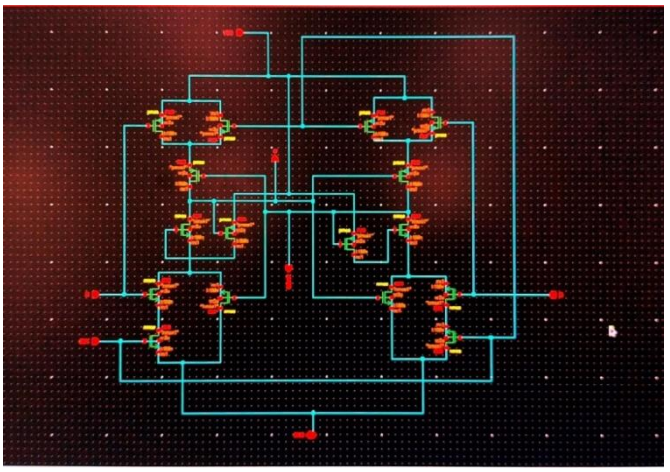

Figure 5 Design of CMOS SR Flip-Flop using ONOFIC

Static power is due to the static state that is no changing state. This is due to the leakage current in the device. Design of CMOS SR Flip-Flop using ONOFIC shown in Figure 5. In OFF states, current continues to flow from VDD to ground, contributing to power dissipation. The reduction of

transistor geometries is a primary factor leading to various leakage currents and is the main cause of static power consumption. Presently, leakage power constitutes approximately 20-50% of total power consumption, and this percentage is on the rise. Various techniques can be employed to minimize static power, and this paper utilizes the ONOFIC approach as one such technique.

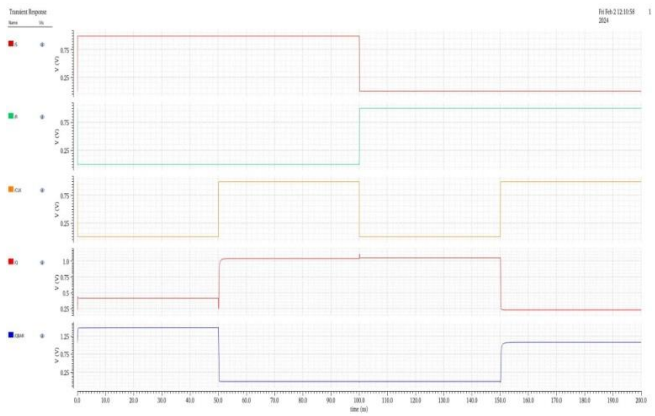

Figure 6 Simulation Result of ONOFIC SR Flip Flop

Tables Analysis of CMOS Power Dissipation

Conventional SR Flip-Flop	2.6 µ
ONOFIC SR Flip-Flop	1.8µ

This section of Table 1 involves a comparative analysis among the traditional CMOS circuits of SR flip-flops & the ONOFIC presentation, specifically focusing on power performance. The outcomes from the ONOFIC are shown in Figure 6 its implementation surpass those obtained from the traditional design.

Conclusion

In this paper has explored with the efficiency and power dissipation of SR flip flop and we have overcome these problems and improved the performance. In the realm of IC design, prioritizing low power is of utmost importance. The ON/OFF (ONOFIC) method discussed above was employed for the design of an SR flip-flop. The simplicity of the ONOFIC technique is notable, employing a single threshold voltage to mitigate leakage current. The primary focus of this approach lies in its enhanced ON/OFF characteristic. Operation of ONOFIC leads to a reduction in leakage power, enhancing the performance of digital circuits—a crucial requirement in the present scenario. A noteworthy outcome of this approach is the resultant low power consumption. Looking ahead, there is potential for further advancements in this approach, particularly if the logic block can be more efficiently turned ON/OFF, conducive to diminishing the propagation delay in logic blocks.

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