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A Modified CSD Conversion for constant multiplication architecture for Air Filter

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Abstract

This paper introduces an efficient hardware architecture for reconfigurable multiple constant multiplication block, based upon canonical signed digit (CSD)-based 4-bit vertical and 8-bit horizontal common sub expression elimination algorithm. The proposed architecture reduces the necessary number of full adder cells and the adder depths in addition to 4-bit specific sub-expressions (CS) in the vertical direction as well as 8-bit CSs in the horizontal direction, leading to reduces operation of adder blocks in comparison with 2-bit and 3-b binary CS elimination. In the first stage conversion of binary coefficients to canonical-signed digit reduce the adder path by lowering non-zero terms present in each coefficient. Further application of MODIFIED CSD conversion algorithm reduces the complexity in multiplicative block by identifying and eliminating the common sub expression leads to decrease in propagation delay with increase in performance of the system.

Key words: canonical-signed digit, Reconfigurable multiple constant multiplication block, non-zero terms, vertical and horizontal common sub expression (VHCSE) algorithm.

1. INTRODUCTION

Modern days applications include software defined radio (SDR) [1], high efficiency video/data coding [2,3] and high rate communication require a reconfiguration in finite impulse response filter hardware structure where the filter's coefficient can be change aggressively. Multiplicative Constant Multiplication (MCM) blocks can comprise of multipliers and adder elements are consider as critical elements, which define the overall performance of filter implementation and hence reconfiguration in Multiplicative Constant Multiplication (MCM) is required to avoid complexity.[4,5] The best choice for the implementation of low complexity FIR is common CSE techniques filter through simple operations like shift-and-add techniques. In this work [5], the power consumption is reduced through turning on/off the multipliers used in FIR filter depends upon multiplier control signal decision.[6-9].The another concept of the Common Sub-expression Elimination is Binary Common Sub-expression Elimination (BCSE) algorithm has been used for designing an FIR. However, the removal of common subexpressions only vertically results in an increase in hardware costs. [7,9].The implementation of Reconfigurable Multiplicative Constant Multiplication based on CSD and VHCSE algorithm which leads to reduce number of full adder cells and adder depth by converting the binary coefficient to CSD at the first stage followed by 4-bit common sub-expression elimination (CSE) vertically followed 8-bit CSE horizontally for reducing the power consumption significantly by reducing the average switching

activities of the adder blocks in RMCM block.[10]. The salient features of the proposed work may be summarized as follows. 1) Reconfigurable architecture of the RMCM hardware based on CSD based VHCSE algorithm, 2) Diminished full adder cell requirements and adder depth for the desired FIR filter by converting the CSD binary in the first step, followed by 4-bit, vertically eliminating and 8-bit CSE at the next stage. 3) The proposed RMCM architecture will decrease energy consumption by increasing the average switching activities of each RMCM module.

2. CONCEPT OF CSD AND BCSE ALGORITHM FOR RMCM DESIGN

2.1 Canonical Signed Digit conversion

Canonical Sign Digit (CSD) is a type of binary number representation and CSD presentation of a binary number consists of numbers 0, 1 and -1. The number of nonzero digits should be minimal and cannot be two consecutive non-zero digits which helps to reduce the number of additions operation required in variable multiplications to reduce the adder depth and switching activity. The recent method used for conversion of binary to CSD conversion based upon the carry by-pass signal [5].The implementation of CSD conversion with the bit-parallel implementation and is shown in Fig. 1.

2.2 Binary Common Sub expression elimination

BCSE algorithm which deals with the elimination of unneeded binary common sub-expression (BCS) that occur within the coefficients of the FIR filter.

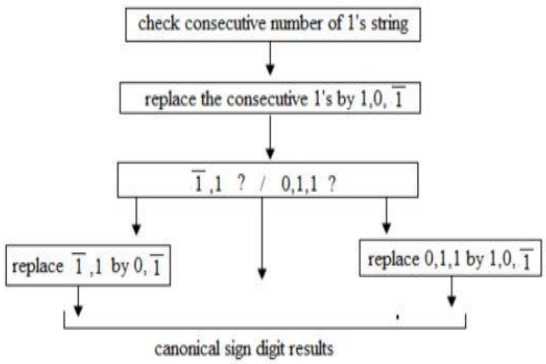

Fig.1.Implementation of CSD conversion with bit parallel implementation.

The BCSE technique focuses on eliminating unnecessary computations in multipliers coefficient by reusing the binary bit patterns (BCS) present in coefficients [10]. An n-bit binary number can form 2n-(n + 1) BCS with in the coefficients.

2.3 Vertical and Horizontal common sub expression elimination

A VHCSE-algorithm was developed based on CSD-decoded coefficients that include vertical (VCS) and horizontal (VCS) 4-bit CSs. The architecture was used to refine coefficient-multiplier hardware (HCS) as depicted graphically in Fig. 3. However, the CSD represented filter coefficients cannot be used as the input to the hardware. Therefore, the coefficients of filter have been partitioned into two tables: magnitude table and sign table which corresponding to the magnitude and the sign bits respectively [14].Next, the 4-bit and 8-bit horizontal and vertical CSs have been applied within the coefficient of filter for reduction of the full adder cell required shift-add based multiplier design. Flow-chart of the proposed CSD-VHCSE algorithm based RMCM design is shown in fig.2.

3. PROBLEM STATEMENT AND PROPOSED SOLUTION

1) While implementing a RMCM block, by considering the signed binary format for representing coefficient increases the number of NZT for each of the coefficient which further leads to increasing number of adders for summing up the partial products. Flow-chart of the proposed CSD-VHCSE algorithm based RMCM design Shown in fig.2.According to the BCSE algorithms [1]–[4], 3-bit and 2-bit BCS in vertical direction increases the number of adders used for summing up the partial product for each of the multiplier. For example, 16-bitcoefficientrequires 5 and 7 adders for single coefficient multiplier using 3-bit and 2-bit BCSE algorithms respectively. Therefore, implementation of 20 tap reconfigurable FIR filter requires total 5 × 20 = 100 and 7 ×20 = 140 adders for 3-bit and 2-bit BCSE algorithms respectively.

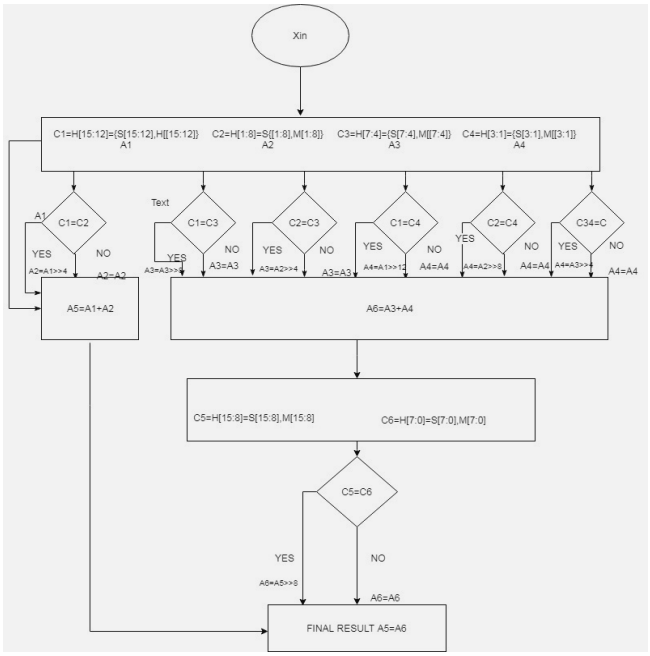

Fig.2. Flow-chart of the proposed CSD-VHCSE algorithm based RMCM design

3.1 Proposed solution

In the proposed method the representation of CSD has been used instead of bilateral representation which helps to reduce the number of NZTs present within a coefficient by more than 50 per cent. The above problem is overcome by considering the following features. The adder depth and adder costs are reduced. It depends upon implementation of CSD based VHCSE algorithm. Fig. 3 shows the architectural description of the reconfigurable multiplicative block. The implementation of architecture considers 16-bit for both the input (Xin) and each filter coefficient. Data flow diagram of the proposed RMCM architecture Shown in fig.3.

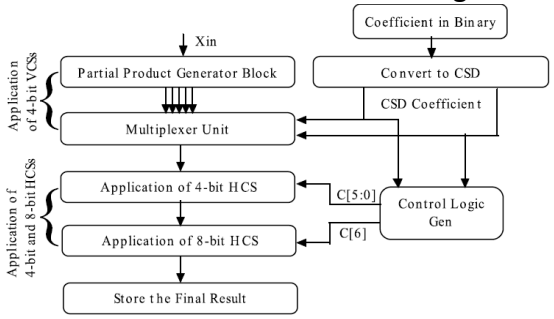

Fig. 3. Data flow diagram of the proposed RMCM architecture

3.2. Binary-to-Canonical Signed Digit Converter Block:

This block performs the conversion of coefficient represented in the signed binary form to the CSD representation and a new carry bypass technique has been found to be suitable for reducing the area as well as the delay. In the current design, the binary-to-CSD converter architecture based on carry bypassing scheme has been adopted and shown in Fig. 4[9].

In this architecture, one processing element (PE) can consists of three-consecutive bits of the filter coefficient (H) are scanned from left-to-right for effective conversion of binary to CSD. Binary-to-CSD recoding scheme using carry bypass signal Shown in fig.4

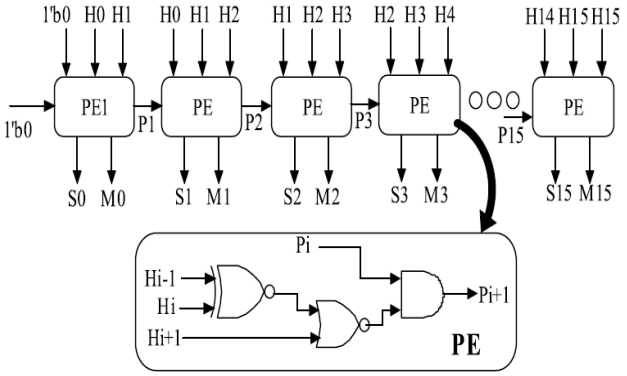

Fig. 4. Binary-to-CSD recoding scheme using carry bypass signal.

3.3 Partial Product Generator

Different partial products (PPs) have been generated based on the size of the binary common sub-expressions and the proposed algorithm, at first the 4-bit vertical CSs decrease the number of adders by eliminating the common operations involved. However, the CSD decoded coefficients cannot be directly represented in binary as two different bit values as involved i.e. sign bit and magnitude bit for a single CSD decoded bit. The negative partial products (P6-P10) have been produced by 2's complementing the original PPs (P1-P5) respectively architectural block description of the partial product generator block is shown in Fig.5

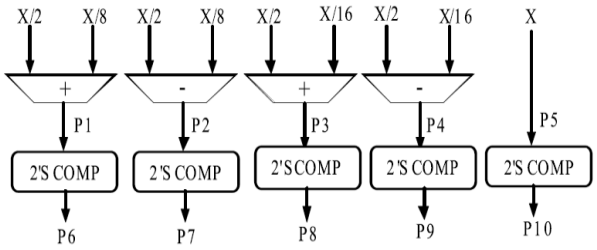

Fig.5. Architecturee of the partial product generator

3.4 Control Signal Generator

Proposed VHCSE algorithm adder's depth can be reduced by applying 4-bit and 8-bit CSs horizontal and vertical direction and each coefficient of 16-bit has been partitioned into four groups, each consisting of 4-bits each and then compared in agreement with the algorithm described in Section II. for finding and eliminating common binary terms present amongst them as shown in Fig. 6. The comparator blocks initiate control signals (C [5:0]) generation by comparing the sign and magnitude simultaneously and control signal C [6] has also been generated by comparing the sign and magnitude for two groups, containing 8-bits each.Architecture of partial product generator Shown in fig.6.

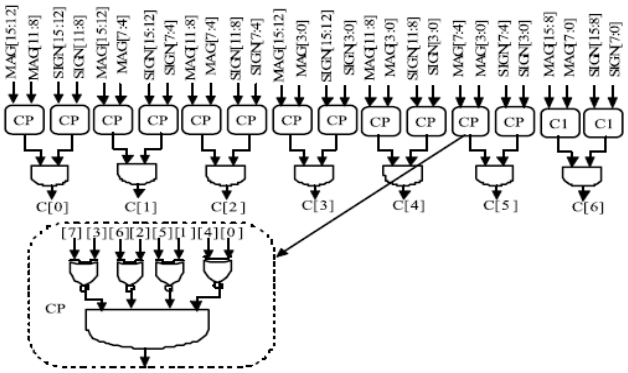

Fig.6.Architecture of partial product generator

4. IMPLEMENTATION AND RESULTS

The coefficients for different FIR filter have been generated and analysis using Xilinx ISE design suite 14.2 design and comparison between carry-bypass and modified CSD conversion have been made. Output waveform for implementation of RMCM block Shown in Fig.7 and Fig.8. Output waveform for carry-bypass signal Shown in fig.8.and Fig.9. Output waveform for without carry-bypass signal Shown in Fig.10

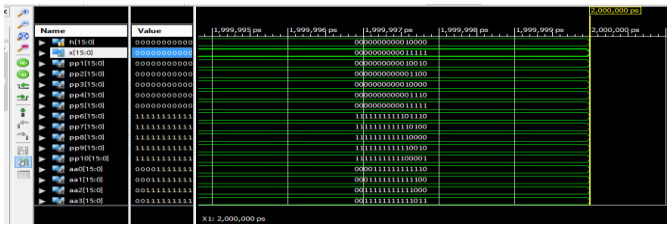

Fig.7. Output waveform for implementation of RMCM block

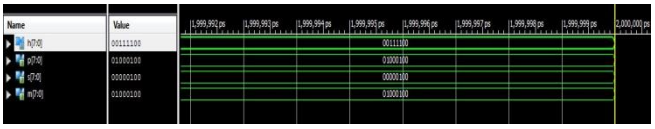

Fig.8. Output waveform for carry-bypass signal

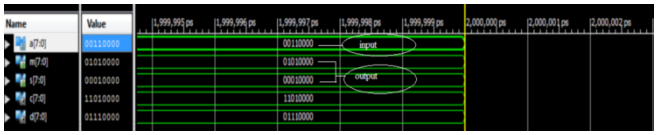

Fig.9. Output waveform for without carry-bypass signal

Comparison between existing method and modified method is shown in table 1 below:

Table.1. Comparison between existing method and modified method

	Existing method	**Modified method**
Area	299 Kilobytes	199 Kilobytes
Power	7375 nw	6702 nw
Delay	1516 ns	846 ns
Memory usage	528788 Kilobytes	560404 Kilobytes

Conclusion

The implementation of method of low-complexity reconfigurable FIR filter synthesis technique for realizing an efficient RMCM block based on the CSD VHCSE algorithm. First, coefficients from the signed decimal format to the canonical signed digit format helps in reducing the complexity of the required full adder cell and adder depth by lowering the number of NZT present in each coefficient. VHCSE algorithm applied on the CSD represented coefficient helps further in reducing the adder depth and complexity of the filter coefficients by finding and eliminating the common sub-expression and improvements in the logic complexity and propagation delay can be achieved by implementation of algorithm.

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